

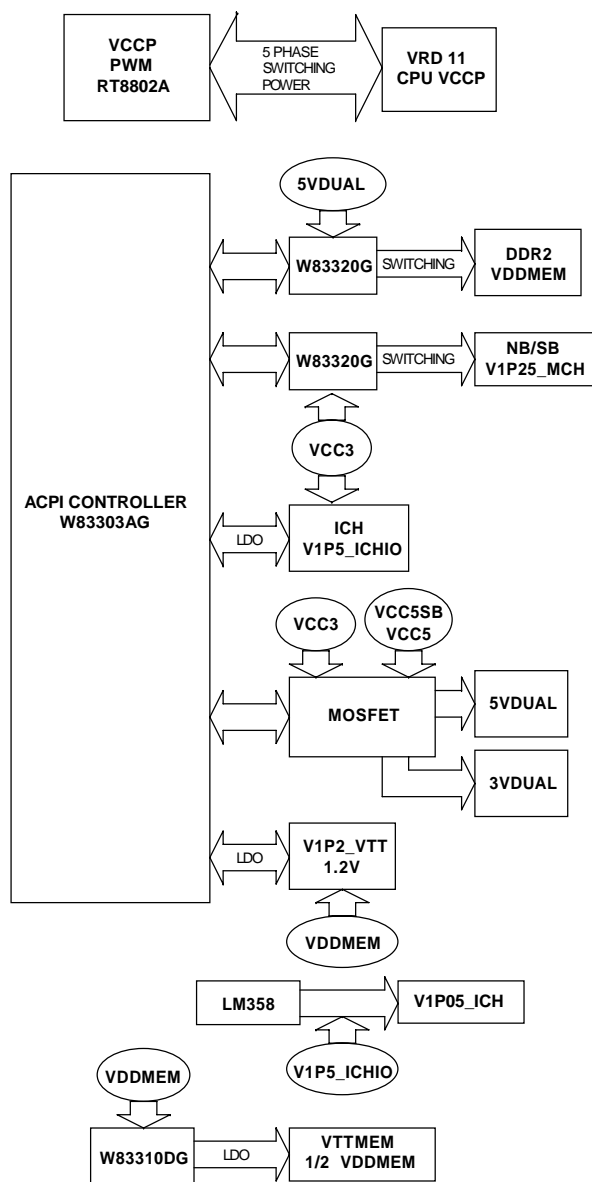
ABIT - M621 SCHEMATICS

Version: 0.1

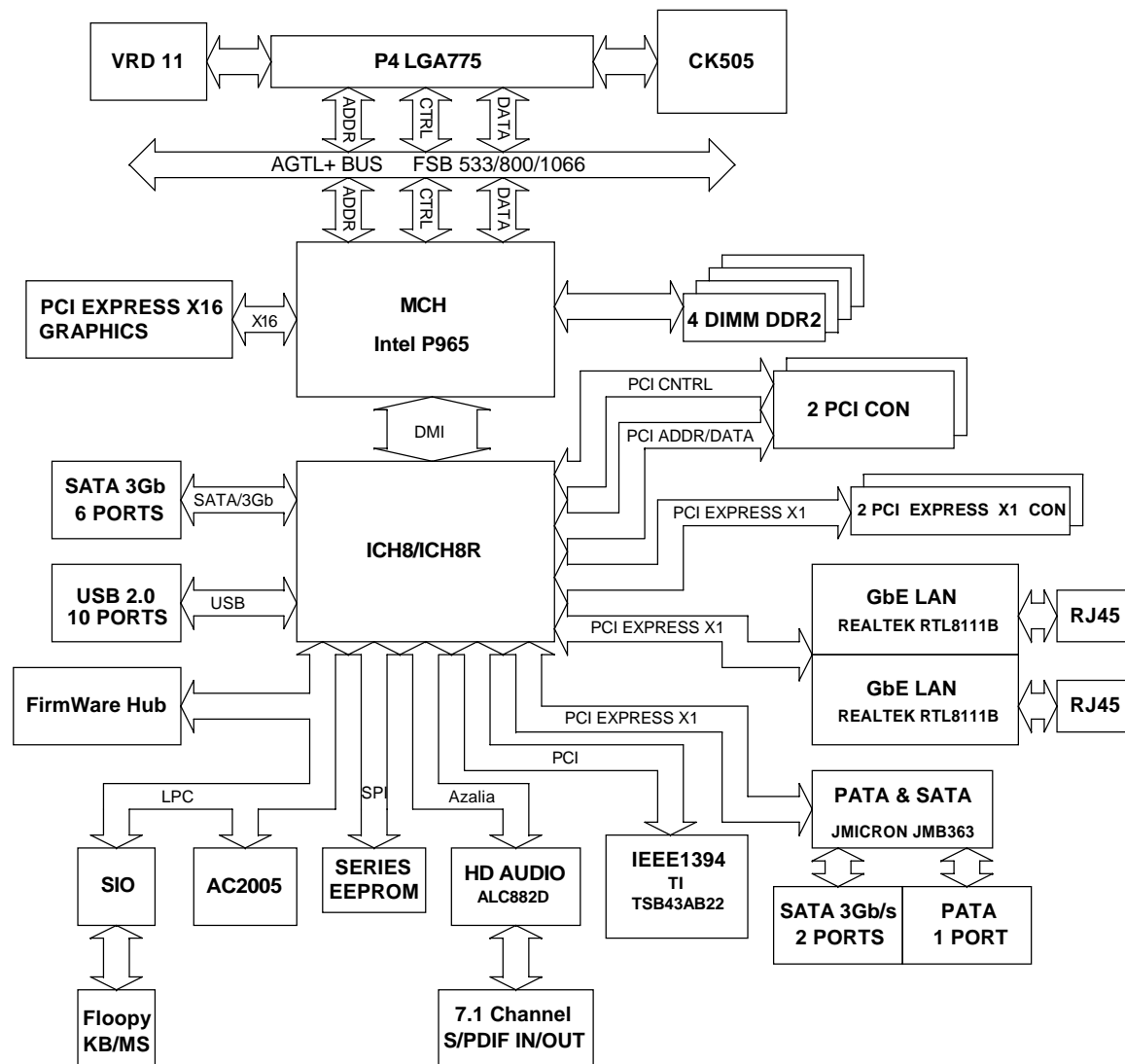
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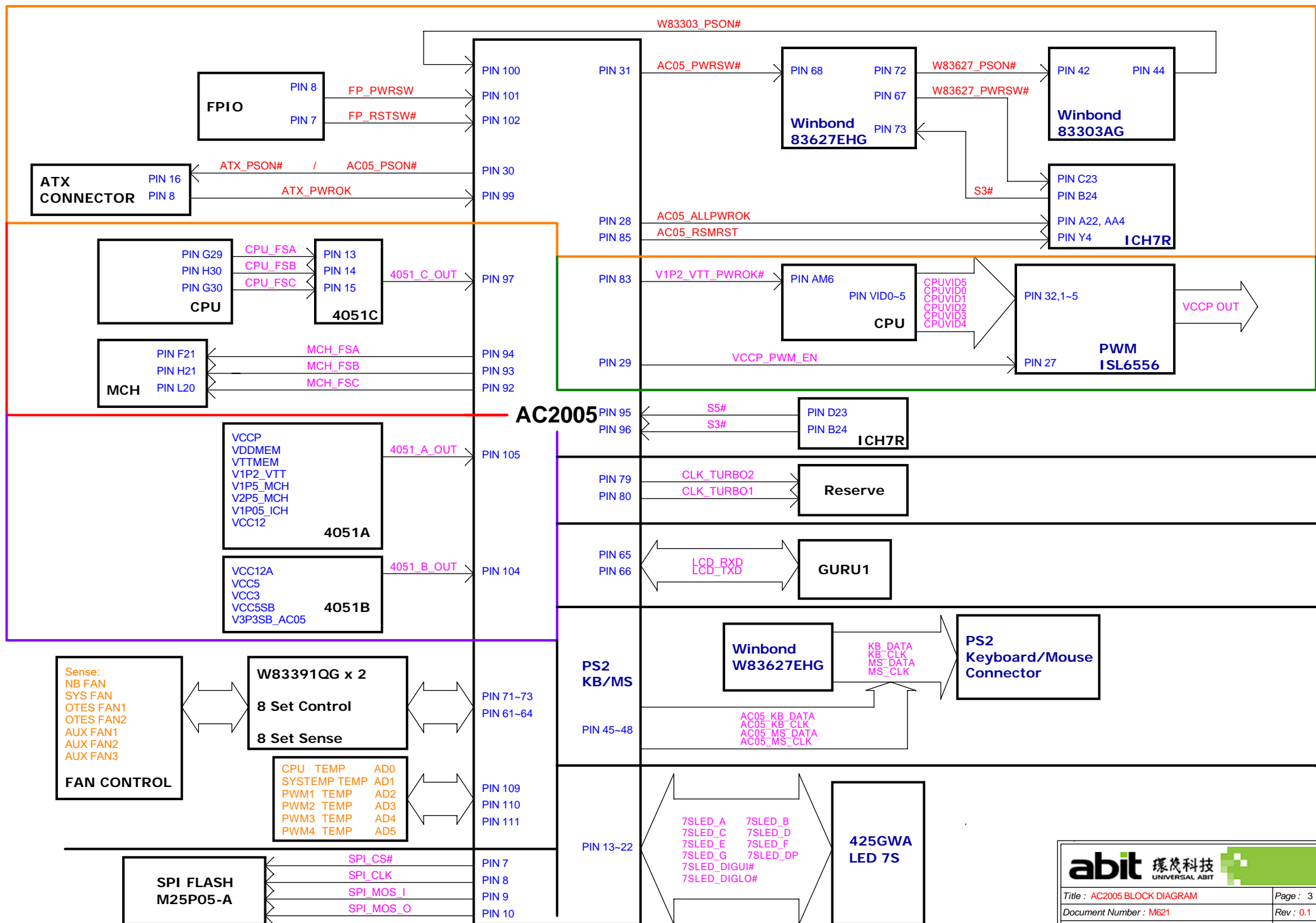
Model	Features
AB9 QuadGT	uGuru, Silent OTES, IEEE1394a, Dual SATA 3Gb/s RAID, Dual PCIE GbE, PATA, 7.1 Channel HD Audio

POWER DESIGN DIAGRAM



BLOCK DIAGRAM





ICH8 GPIO SETTING

Pin Name	Power Well	Usage	Default
GPIO0	3.3V Core	ACZ_DET	GPI
GPIO1	3.3V Core	TACH1	GPI
GPIO2	5V Core	PIRQ#E	GPI
GPIO3	5V Core	PIRQ#F	GPI
GPIO4	5V Core	PIRQ#G	GPI
GPIO5	5V Core	PIRQ#H	GPI
GPIO6	3.3V Core	TACH2	GPI
GPIO7	3.3V Core	TACH3	GPI
GPIO8	3.3V Sus	LPC_PME#	GPI
GPIO9	3.3V Sus	WOL_EN	Native
GPIO10	3.3V Sus	LAN2_WAKE#	GPI
GPIO11	3.3V Sus	SMBALERT#	Native
GPIO12	3.3V Sus	LAN1_WAKE#	GPI
GPIO13	3.3V Sus	1394_PME#	GPI
GPIO14	3.3V Sus	CLGPIO2	GPI
GPIO15	3.3V Sus	STP_PCI#	Native
GPIO16	3.3V Core	FWH_WP#	GPO
GPIO17	3.3V Core	TACH0	GPI
GPIO18	3.3V Core	GPIO18	GPO
GPIO19	3.3V Core	SATA1GP	GPI
GPIO20	3.3V Core	GPIO20	GPO
GPIO21	3.3V Core	SATA0GP	GPI
GPIO22	3.3V Core	SCLOCK	Native
GPIO23	3.3V Core	LDRQ1#	Native
GPIO24	3.3V Sus	CLGPIO0	GPO
GPIO25	3.3V Sus	STP_CPU#	Native
GPIO26	3.3V Sus	S4_STATE#	GPO
GPIO27	3.3V Sus	EL_STATE0	GPO
GPIO28	3.3V Sus	EL_STATE1	GPO
GPIO29	3.3V Sus	OC5#	Native
GPIO30	3.3V Sus	OC6#	Native
GPIO31	3.3V Sus	OC7#	Native
GPIO32	3.3V Core	GIPO32	GPO
GPIO33	3.3V Core	BORAD ID	GPO
GPIO34	3.3V Core	BOARD ID	GPO
GPIO35	3.3V Core	SATACLKREQ#	GPO
GPIO36	3.3V Core	SATA2GP	GPI
GPIO37	3.3V Core	SATA3GP	GPI
GPIO38	3.3V Core	SLOAD	GPI
GPIO39	3.3V Core	SDATAOUT0	GPI
GPIO40	3.3V Sus	OC1#	Native
GPIO41	3.3V Sus	OC2#	Native
GPIO42	3.3V Sus	OC3#	Native
GPIO43	3.3V Sus	OC4#	Native
GPIO44~47	N/A	Not implemented	N/A
GPIO48	3.3V Core	SDATAOUT0	GPI
GPIO49	V_CPU_IO	CPUPWRGD	Native
GPIO50	5.5V Core	REQ1#	Native
GPIO51	3.3V Core	GNT1#	Native
GPIO52	5.5V Core	REQ2#	Native
GPIO53	3.3V Core	GNT2#	Native
GPIO54	5.5V Core	REQ3#	Native
GPIO55	3.3V Core	GNT3#	Native

W83303AG Voltage Adjust Table

a.CR03 (Linear Regulatio Voltage Setting Register, Default 0x00h, Read/Write)

Bit2	Bit1	Bit0	V1P25_MCH
0	0	0	+0%
0	0	1	+2%
0	1	0	+4%
0	1	1	+8%
1	0	0	+12%
1	0	1	+16%

b.CR02(VRAM Voltage Setting Register,Default x000 0000b,Read/Write)

Bit 7 is reserved for signal DDRDET# setting (Dynamic Detect)

DDRDET# = HIGH bit7 = 1 DDR II type

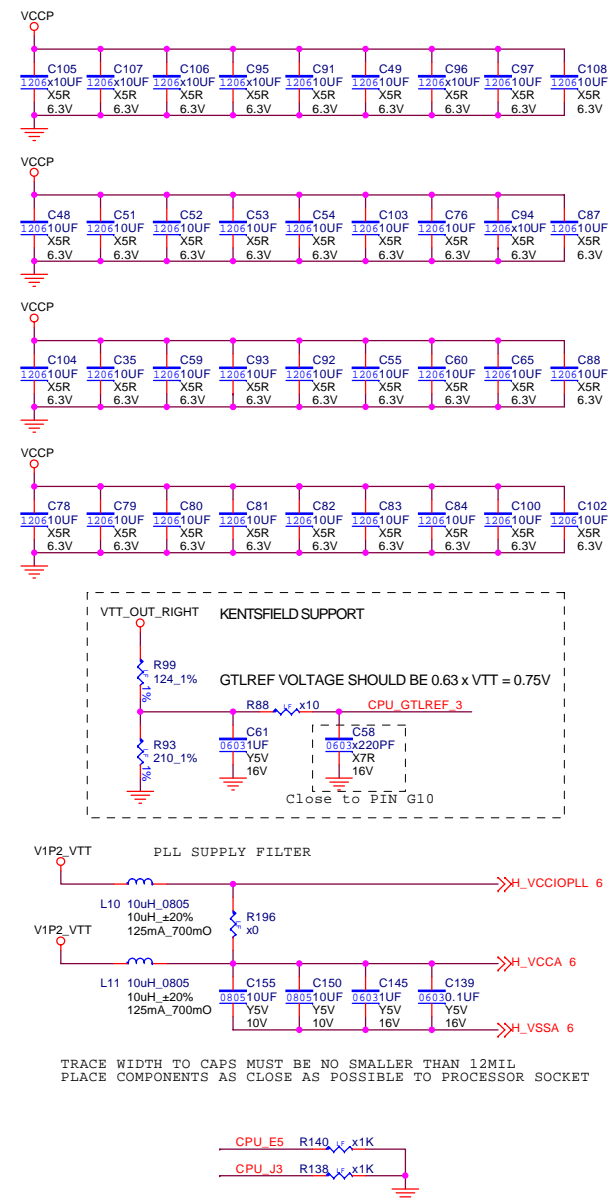
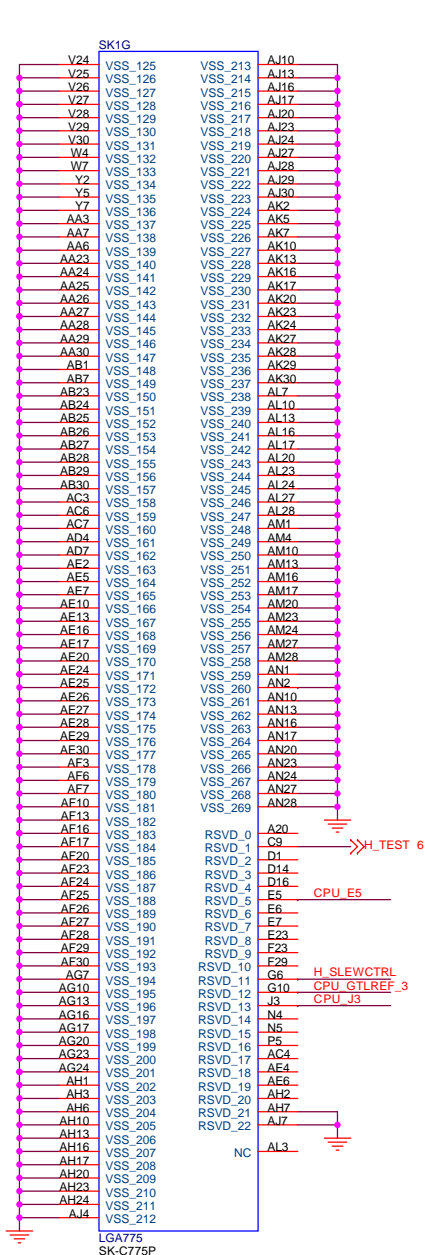
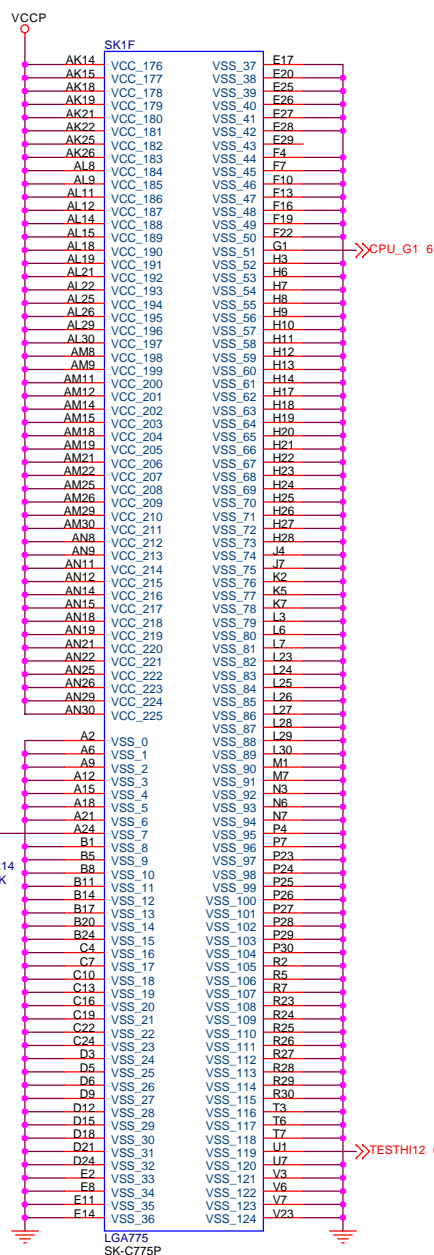
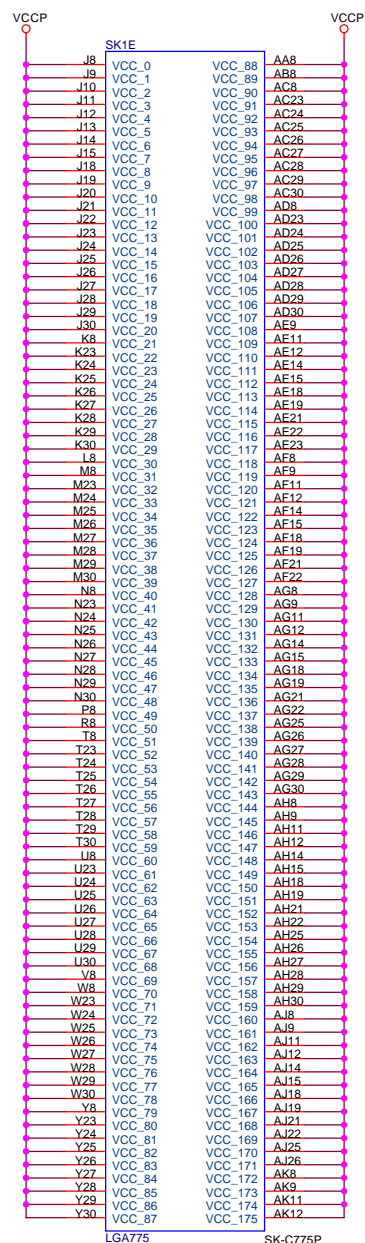
Low bit7 = 0 DDR type

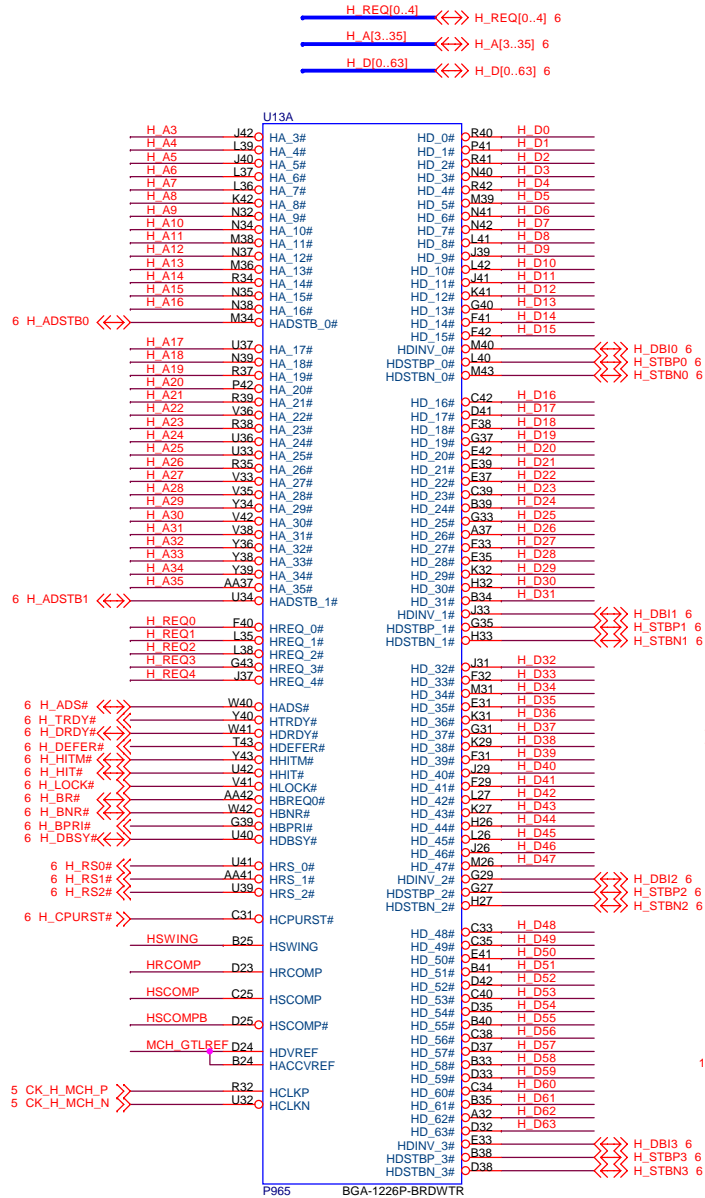
Bit7	Bit3	Bit2	Bit1	Bit0	VDDMEM
1	0	0	0	0	1.80V
1	0	0	0	1	1.75V
1	0	0	1	0	1.85V
1	0	0	1	1	1.90V
1	0	1	0	0	1.95V
1	0	1	0	1	2.00V
1	0	1	1	0	2.05V
1	0	1	1	1	2.10V
1	1	0	0	0	2.20V
1	1	0	0	1	2.30V

PCI DEVICE SETTING

DEVICE	PCI1	PCI2	1394
INTA	F	H	B
INTB	G	E	
INTC	H	F	
INTD	E	G	
IDSEL	21	22	18
REQ/GNT	1	2	0







M_MAA_A[0..14] 11,13
M_DQS_P_A[0..7] 11
M_DQS_N_A[0..7] 11
M_DATA_A[0..63] 11

M_MAA_B[0..14] 12,13
M_DQS_P_B[0..7] 12
M_DQS_N_B[0..7] 12
M_DATA_B[0..63] 12

M_MAA_B[0..14] 12,13
M_DQS_P_B[0..7] 12
M_DQS_N_B[0..7] 12
M_DATA_B[0..63] 12

M_MAA_B[0..14] 12,13
M_DQS_P_B[0..7] 12
M_DQS_N_B[0..7] 12
M_DATA_B[0..63] 12

U13D
M_MAA_A0 BA31 SMA_A_0 SDQS_A_0
M_MAA_A1 BB25 SMA_A_1 SDQS_A_0#
M_MAA_A2 BA26 SMA_A_2 SDM_A_0
M_MAA_A3 BA25 SMA_A_3 SDQ_A_0
M_MAA_A4 AY26 SMA_A_4 SDQ_A_1
M_MAA_A5 BA23 SMA_A_5 SDQ_A_2
M_MAA_A6 AY24 SMA_A_6 SDQ_A_3
M_MAA_A7 AY23 SMA_A_7 SDQ_A_4
M_MAA_A8 BB23 SMA_A_8 SDQ_A_5
M_MAA_A9 BA22 SMA_A_9 SDQ_A_6
M_MAA_A10 AY33 SMA_A_10 SDQ_A_7
M_MAA_A11 BB22 SMA_A_11 SDQS_A_7#
M_MAA_A12 AW21 SMA_A_12 SDQS_A_1#
M_MAA_A13 AY38 SMA_A_13 SDM_A_1
M_MAA_A14 BA21 SMA_A_14 SDQ_A_8
11,13 M_WE_A BB34 SWE_A# SDQ_A_9
11,13 M_CAS_A AY35 SCAS_A# SDQ_A_10
11,13 M_RAS_A BB33 SRAS_A# SDQ_A_11
11,13 M_SBA_A0 BA33 SBS_A_0 SDQ_A_12
11,13 M_SBA_A1 AW32 SBS_A_1 SDQ_A_13
11,13 M_SBA_A2 BB21 SBS_A_2 SDQ_A_14
11,13 M_SCS_A0 AW35 SCS_A_0# SDQ_A_15
11,13 M_SCS_A1 BA35 SCS_A_1# SDQS_A_2
11,13 M_SCS_A2 BA34 SCS_A_2# SDM_A_2
11,13 M_SCS_A3 BB38 SCS_A_3# SDQ_A_16
11,13 M_SCKE_A0 BC20 SCKE_A_0 SDQ_A_17
11,13 M_SCKE_A1 AY20 SCKE_A_1 SDQ_A_18
11,13 M_SCKE_A2 AY21 SCKE_A_2 SDQ_A_19
11,13 M_SCKE_A3 BA19 SCKE_A_3 SDQ_A_20
11,13 M_SODT_A0 AY37 SODT_A_0 SDQ_A_21
11,13 M_SODT_A1 BA38 SODT_A_1 SDQ_A_22
11,13 M_SODT_A2 BB35 SODT_A_2 SDQ_A_23
11,13 M_SODT_A3 BA39 SODT_A_3 SDQS_A_3#
11 CK_M_DDR_P_A0 AU31 SCLK_A_0 SDQ_A_24
11 CK_M_DDR_N_A0 AR31 SCLK_A_0# SDQ_A_25
11 CK_M_DDR_P_A1 AP27 SCLK_A_1 SDQ_A_26
11 CK_M_DDR_N_A1 AN27 SCLK_A_1# SDQ_A_27
11 CK_M_DDR_P_A2 AV33 SCLK_A_2 SDQ_A_28
11 CK_M_DDR_N_A2 AW33 SCLK_A_2# SDQ_A_29
11 CK_M_DDR_P_A3 AP29 SCLK_A_3 SDQ_A_30
11 CK_M_DDR_N_A3 AP31 SCLK_A_3# SDQ_A_31
11 CK_M_DDR_P_A4 AM26 SCLK_A_4 SDQS_A_4
11 CK_M_DDR_N_A4 AM27 SCLK_A_4# SDQS_A_4#
11 CK_M_DDR_P_A5 AT33 SCLK_A_5 SDQ_A_32
11 CK_M_DDR_N_A5 AU33 SCLK_A_5# SDQ_A_33
SDQS_A_34
SDQ_A_35
SDQ_A_36
SDQ_A_37
SDQ_A_38
SDQ_A_39
SDQS_A_5#
SDQS_A_5#
SDM_A_5
SDQ_A_40
SDQ_A_41
SDQ_A_42
SDQ_A_43
SDQ_A_44
SDQ_A_45
SDQ_A_46
SDQ_A_47
SDQS_A_6
SDQS_A_6#
SDM_A_6
SDQ_A_48
SDQ_A_49
SDQ_A_50
SDQ_A_51
SDQ_A_52
SDQ_A_53
SDQ_A_54
SDQ_A_55
SDQS_A_7
SDQS_A_7#
SDM_A_7
SDQ_A_56
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SDQ_A_61
SDQ_A_62
SDQ_A_63

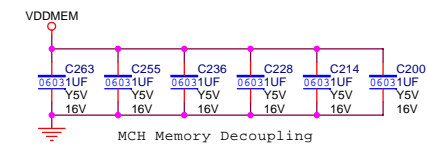
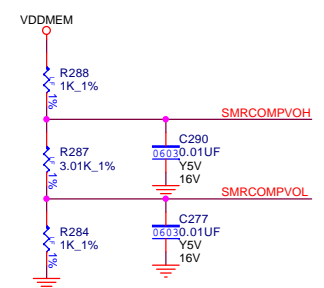
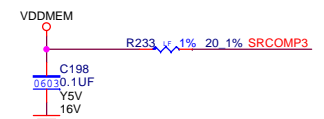
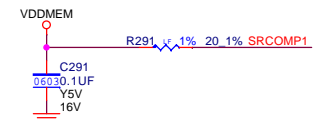
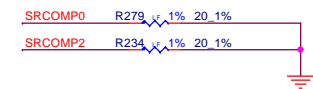
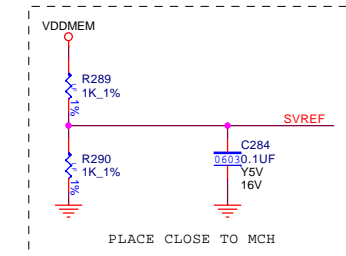
P965 BGA-1226P-BRDWTR

U13E
M_MAA_B0 BB17 SMA_B_0 SDQS_B_0
M_MAA_B1 AY17 SMA_B_1 SDQS_B_0#
M_MAA_B2 BA17 SMA_B_2 SDM_B_0
M_MAA_B3 BC16 SMA_B_3 SDQ_B_0
M_MAA_B4 AW15 SMA_B_4 SDQ_B_1
M_MAA_B5 BB15 SMA_B_5 SDQ_B_2
M_MAA_B6 BA14 SMA_B_6 SDQ_B_3
M_MAA_B7 AY15 SMA_B_7 SDQ_B_4
M_MAA_B8 BB14 SMA_B_8 SDQ_B_5
M_MAA_B9 AW14 SMA_B_9 SDQ_B_6
M_MAA_B10 BB13 SMA_B_10 SDQ_B_7
M_MAA_B11 BA13 SMA_B_11 SDQS_B_1#
M_MAA_B12 AY29 SMA_B_12 SDQS_B_1#
M_MAA_B13 BB13 SMA_B_13 SDM_B_1
M_MAA_B14 AY13 SMA_B_14 SDQ_B_8
11,13 M_WE_B BB27 SWE_B# SDQ_B_9
11,13 M_CAS_B AY29 SCAS_B# SDQ_B_10
11,13 M_RAS_B BB26 SRAS_B# SDQ_B_11
11,13 M_SBA_B0 BA27 SBS_B_0 SDQ_B_12
11,13 M_SBA_B1 BB18 SBS_B_1 SDQ_B_13
11,13 M_SBA_B2 BC12 SBS_B_2 SDQ_B_14
11,13 M_SCS_B0 BB27 SCS_B_0# SDQ_B_15
11,13 M_SCS_B1 BB30 SCS_B_1# SDQS_B_2
11,13 M_SCS_B2 AY27 SDM_B_2
11,13 M_SCS_B3 AY31 SDQ_B_16
11,13 M_SCKE_B0 AY12 SCKE_B_0 SDQ_B_17
11,13 M_SCKE_B1 BB11 SCKE_B_1 SDQ_B_18
11,13 M_SCKE_B2 BA11 SCKE_B_2 SDQ_B_19
11,13 M_SCKE_B3 BA29 SCKE_B_3 SDQ_B_20
11,13 M_SODT_B0 BA29 SODT_B_0 SDQ_B_21
11,13 M_SODT_B1 BA30 SODT_B_1 SDQ_B_22
11,13 M_SODT_B2 BB29 SODT_B_2 SDQ_B_23
11,13 M_SODT_B3 BB31 SODT_B_3 SDQS_B_3#
12 CK_M_DDR_P_B0 AV31 SCLK_B_0 SDQ_B_24
12 CK_M_DDR_N_B0 AW31 SCLK_B_0# SDQ_B_25
12 CK_M_DDR_P_B1 AU27 SCLK_B_1 SDQ_B_26
12 CK_M_DDR_N_B1 AT27 SCLK_B_1# SDQ_B_27
12 CK_M_DDR_P_B2 AV32 SCLK_B_2 SDQ_B_28
12 CK_M_DDR_N_B2 AT32 SCLK_B_2# SDQ_B_29
12 CK_M_DDR_P_B3 AU29 SCLK_B_3 SDQ_B_30
12 CK_M_DDR_N_B3 AR29 SCLK_B_3# SDQ_B_31
12 CK_M_DDR_P_B4 AV29 SCLK_B_4 SDQS_B_4
12 CK_M_DDR_N_B4 AW27 SCLK_B_4# SDQS_B_4#
12 CK_M_DDR_P_B5 AN33 SCLK_B_5 SDQ_B_32
12 CK_M_DDR_N_B5 AP32 SCLK_B_5# SDQ_B_33
SDQS_B_34
SDQ_B_35
SDQ_B_36
SDQ_B_37
SDQ_B_38
SDQ_B_39
SDQS_B_5#
SDQS_B_5#
SDM_B_5
SDQ_B_40
SDQ_B_41
SDQ_B_42
SDQ_B_43
SDQ_B_44
SDQ_B_45
SDQ_B_46
SDQ_B_47
SDQS_B_6
SDQS_B_6#
SDM_B_6
SDQ_B_48
SDQ_B_49
SDQ_B_50
SDQ_B_51
SDQ_B_52
SDQ_B_53
SDQ_B_54
SDQ_B_55
SDQS_B_7
SDQS_B_7#
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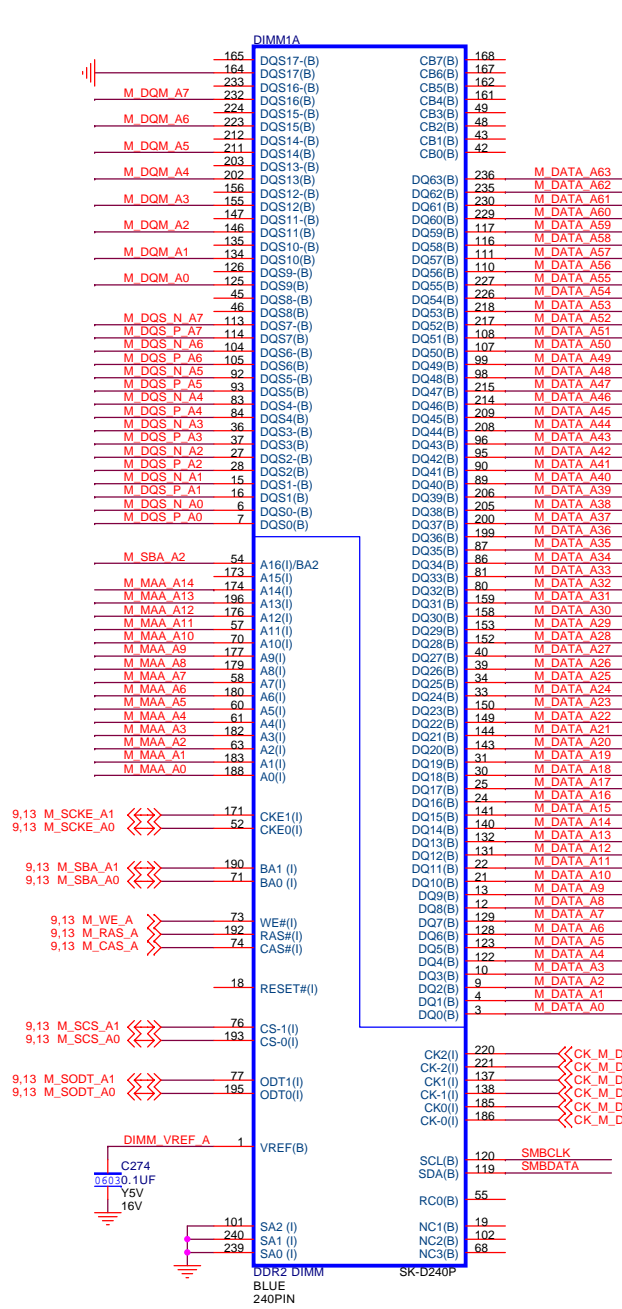
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SRCOMP1 AN3
SRCOMP2 BB40
SRCOMP3 BA40
SMRCOMPVOL AM8
SMRCOMPVOLH AM10

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SRCOMP0 AN2
SRCOMP1 AN3
SRCOMP2 BB40
SRCOMP3 BA40
SMRCOMPVOL AM8
SMRCOMPVOLH AM10

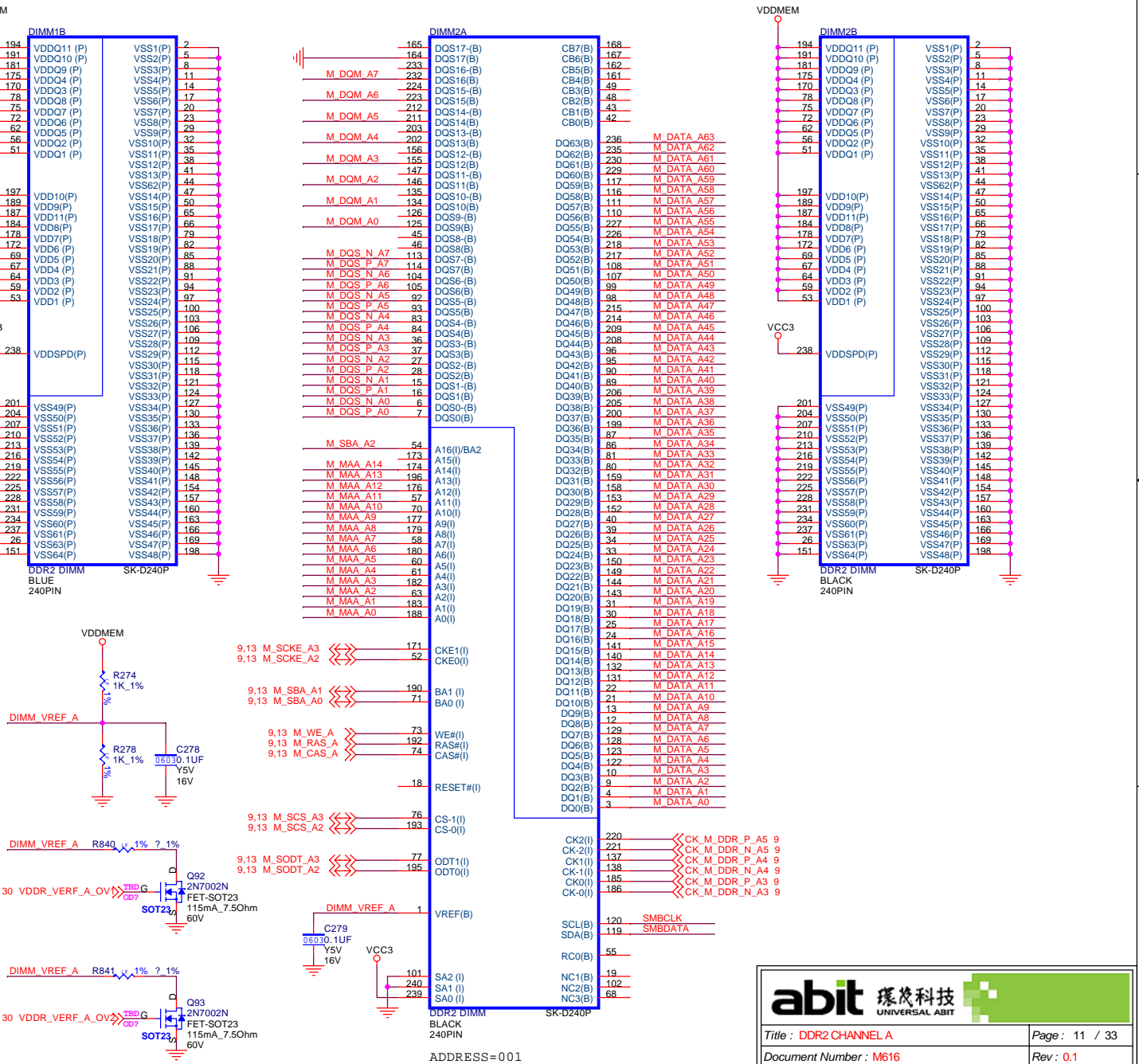
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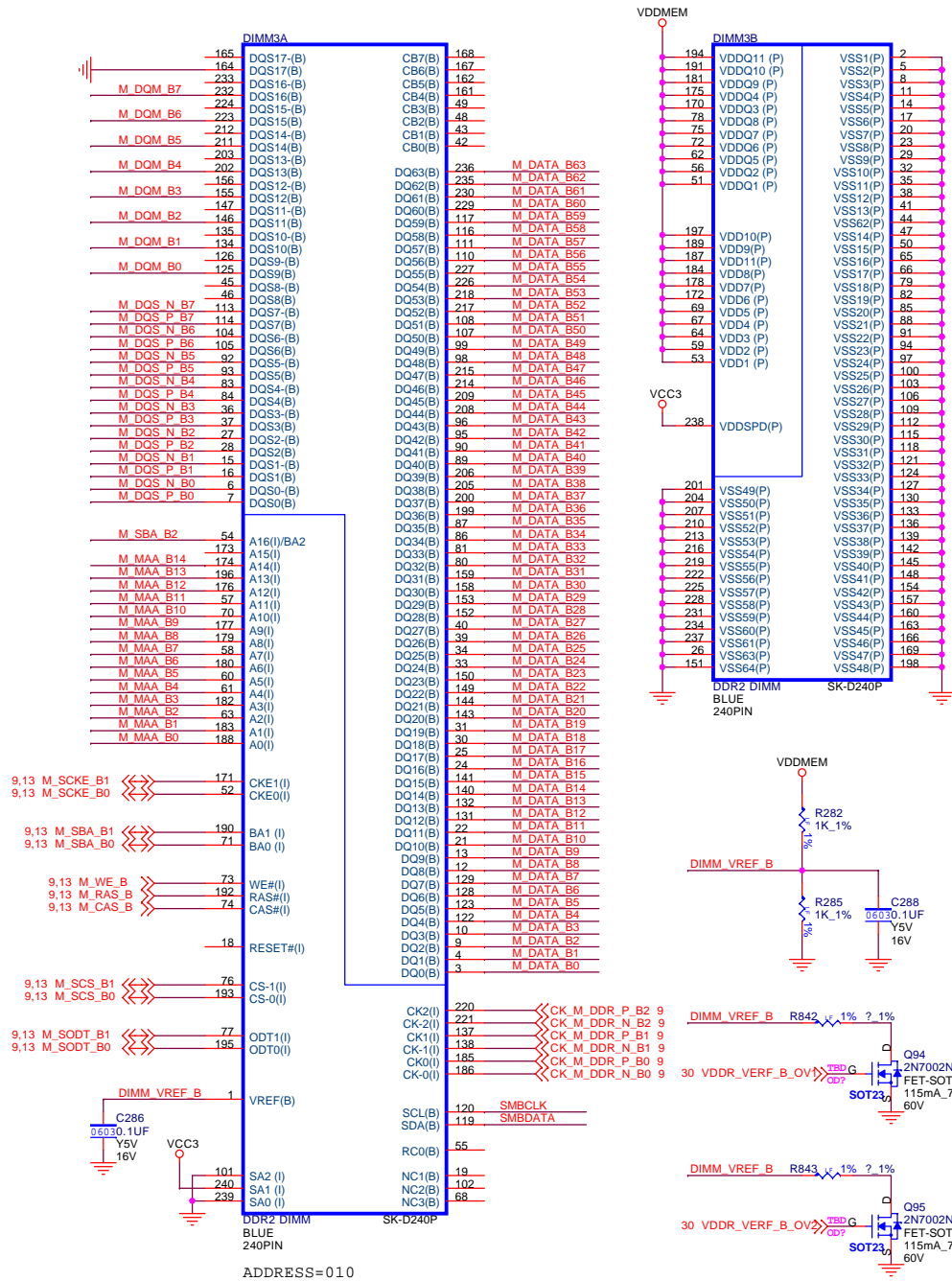
Channel A DIMM1



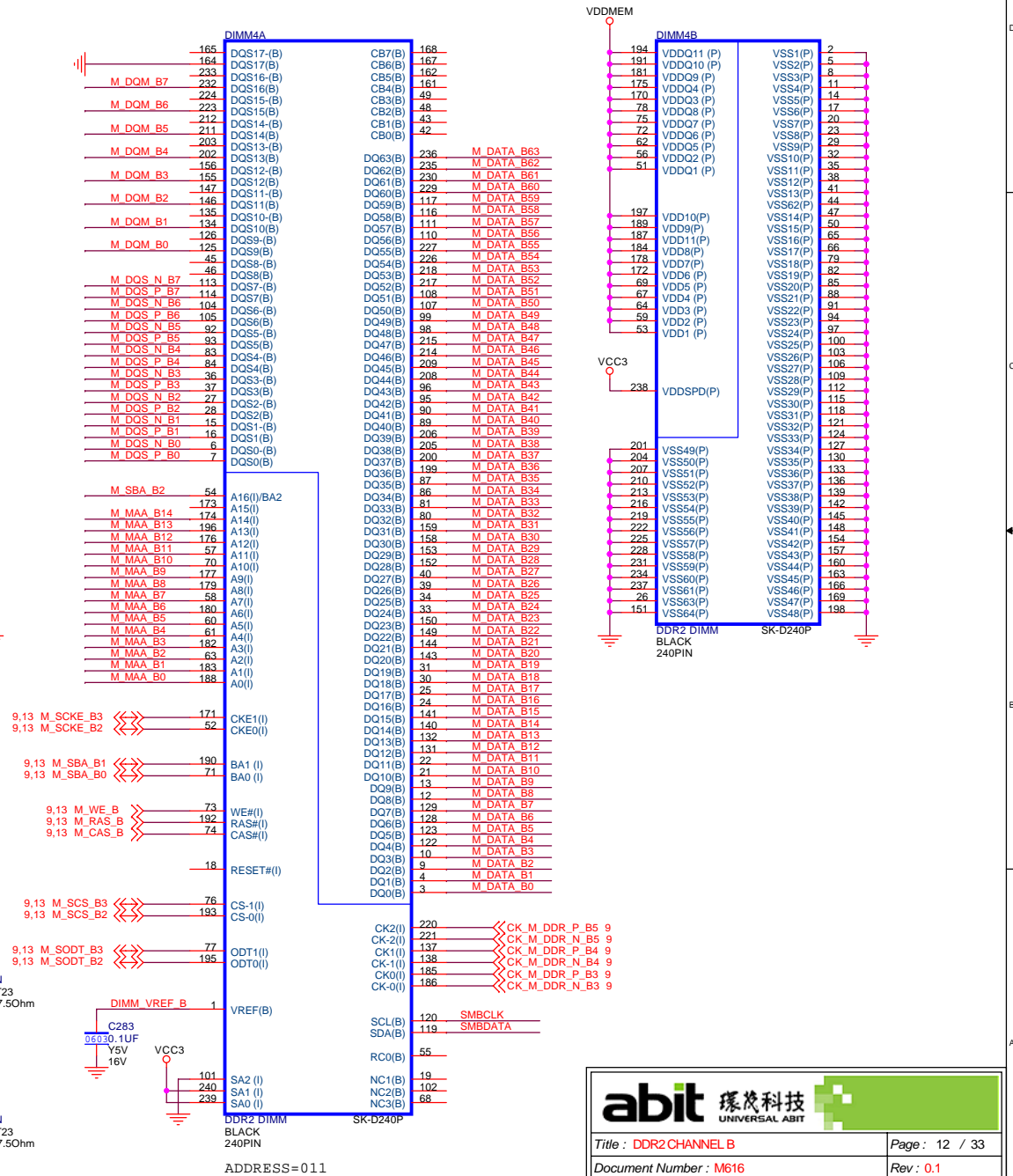
Channel A DIMM2

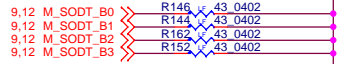
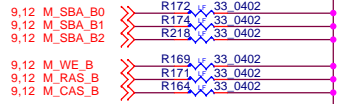
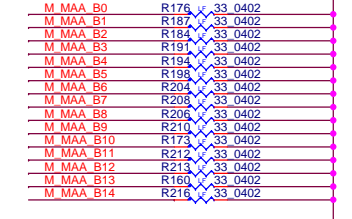
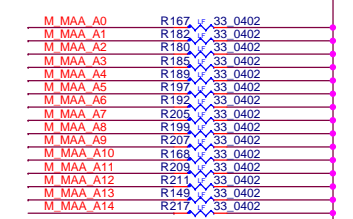
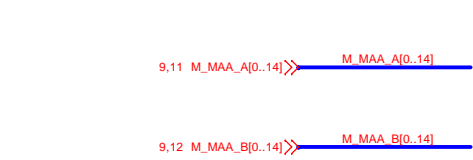
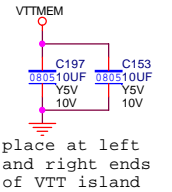
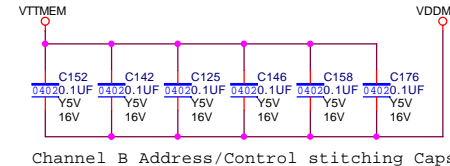
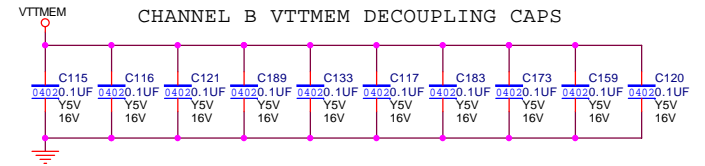
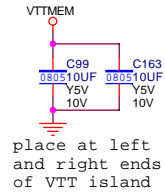
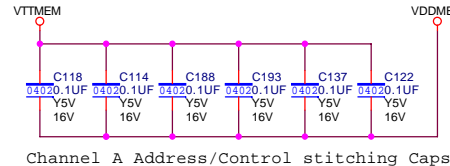
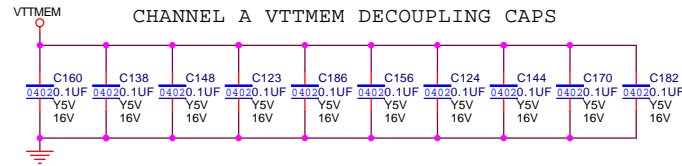
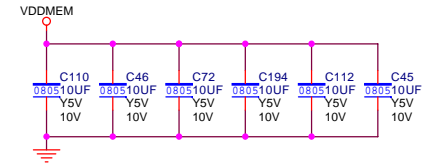
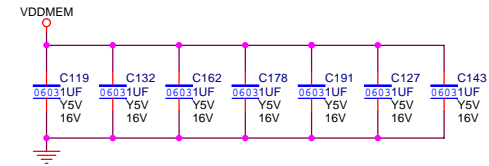
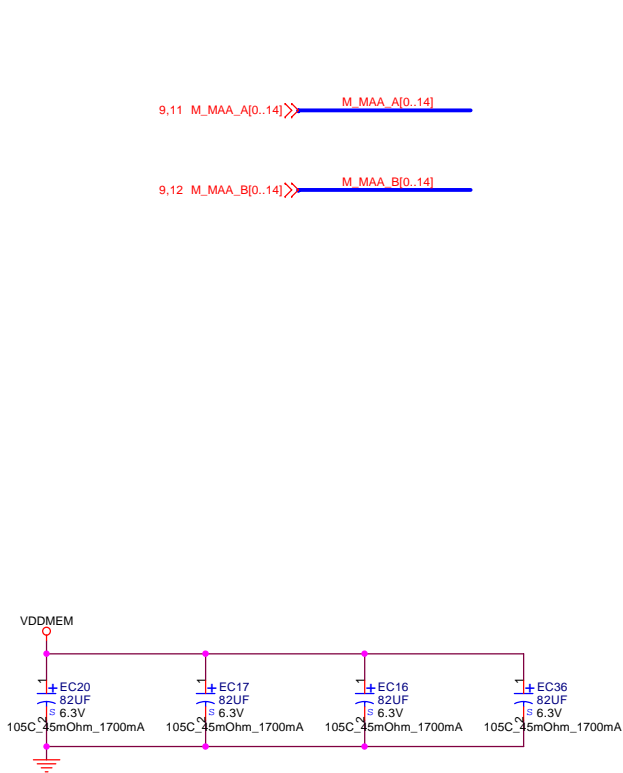


Channel B DIMM1



Channel B DIMM2



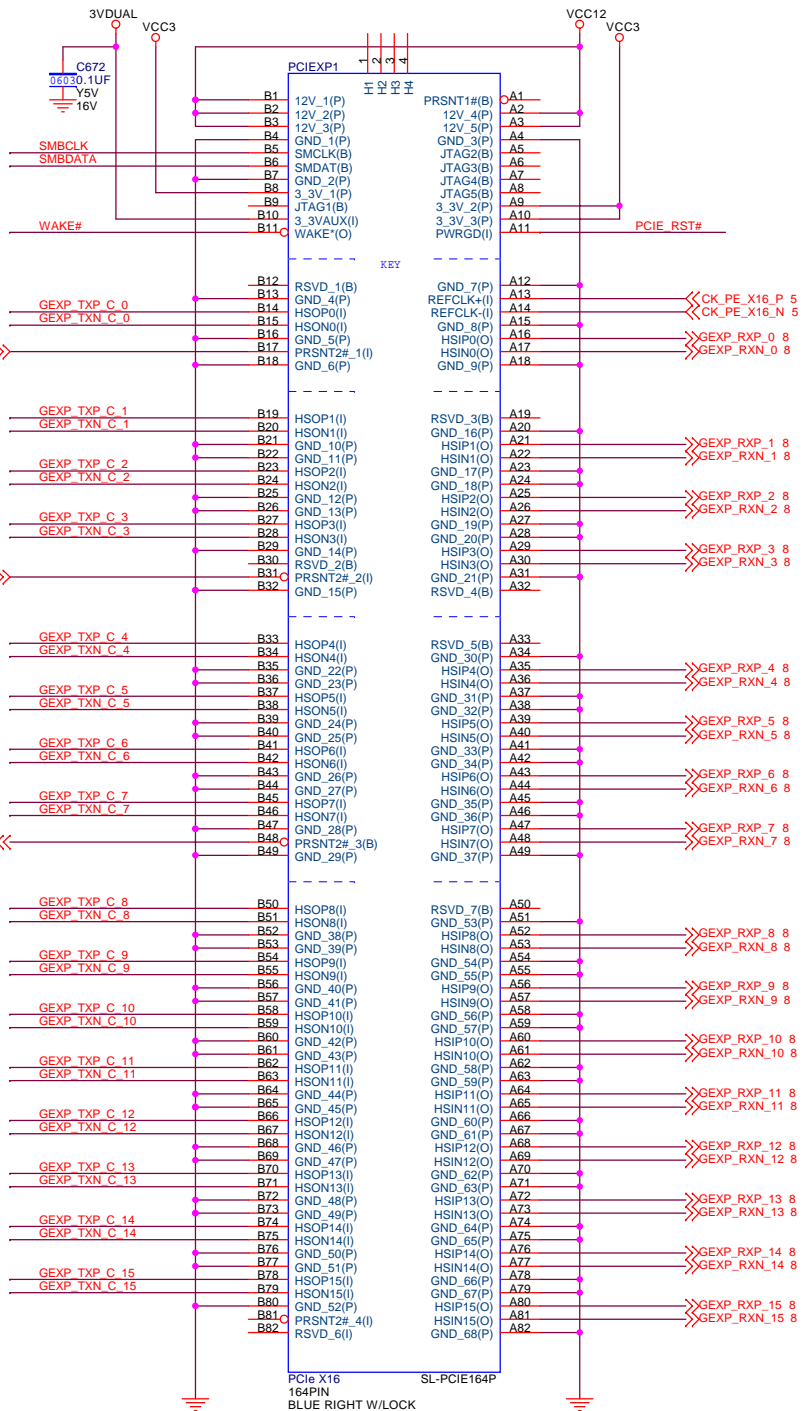


8 GEXP_TXP_0 >> C303 0.1UF GEXP_TXP_C_0
Y5V 16V
8 GEXP_TXN_0 >> C302 0.1UF GEXP_TXN_C_0
Y5V 16V
8 GEXP_TXP_1 >> C304 0.1UF GEXP_TXP_C_1
Y5V 16V
8 GEXP_TXN_1 >> C305 0.1UF GEXP_TXN_C_1
Y5V 16V
8 GEXP_TXP_2 >> C306 0.1UF GEXP_TXP_C_2
Y5V 16V
8 GEXP_TXN_2 >> C307 0.1UF GEXP_TXN_C_2
Y5V 16V
8 GEXP_TXP_3 >> C308 0.1UF GEXP_TXP_C_3
Y5V 16V
8 GEXP_TXN_3 >> C309 0.1UF GEXP_TXN_C_3
Y5V 16V
8 GEXP_TXP_4 >> C310 0.1UF GEXP_TXP_C_4
Y5V 16V
8 GEXP_TXN_4 >> C311 0.1UF GEXP_TXN_C_4
Y5V 16V
8 GEXP_TXP_5 >> C313 0.1UF GEXP_TXP_C_5
Y5V 16V
8 GEXP_TXN_5 >> C312 0.1UF GEXP_TXN_C_5
Y5V 16V
8 GEXP_TXP_6 >> C315 0.1UF GEXP_TXP_C_6
Y5V 16V
8 GEXP_TXN_6 >> C314 0.1UF GEXP_TXN_C_6
Y5V 16V
8 GEXP_TXP_7 >> C317 0.1UF GEXP_TXP_C_7
Y5V 16V
8 GEXP_TXN_7 >> C316 0.1UF GEXP_TXN_C_7
Y5V 16V
8 GEXP_TXP_8 >> C318 0.1UF GEXP_TXP_C_8
Y5V 16V
8 GEXP_TXN_8 >> C319 0.1UF GEXP_TXN_C_8
Y5V 16V
8 GEXP_TXP_9 >> C320 0.1UF GEXP_TXP_C_9
Y5V 16V
8 GEXP_TXN_9 >> C321 0.1UF GEXP_TXN_C_9
Y5V 16V
8 GEXP_TXP_10 >> C323 0.1UF GEXP_TXP_C_10
Y5V 16V
8 GEXP_TXN_10 >> C322 0.1UF GEXP_TXN_C_10
Y5V 16V
8 GEXP_TXP_11 >> C325 0.1UF GEXP_TXP_C_11
Y5V 16V
8 GEXP_TXN_11 >> C324 0.1UF GEXP_TXN_C_11
Y5V 16V
8 GEXP_TXP_12 >> C327 0.1UF GEXP_TXP_C_12
Y5V 16V
8 GEXP_TXN_12 >> C326 0.1UF GEXP_TXN_C_12
Y5V 16V
8 GEXP_TXP_13 >> C329 0.1UF GEXP_TXP_C_13
Y5V 16V
8 GEXP_TXN_13 >> C328 0.1UF GEXP_TXN_C_13
Y5V 16V
8 GEXP_TXP_14 >> C331 0.1UF GEXP_TXP_C_14
Y5V 16V
8 GEXP_TXN_14 >> C330 0.1UF GEXP_TXN_C_14
Y5V 16V
8 GEXP_TXP_15 >> C333 0.1UF GEXP_TXP_C_15
Y5V 16V
8 GEXP_TXN_15 >> C332 0.1UF GEXP_TXN_C_15
Y5V 16V

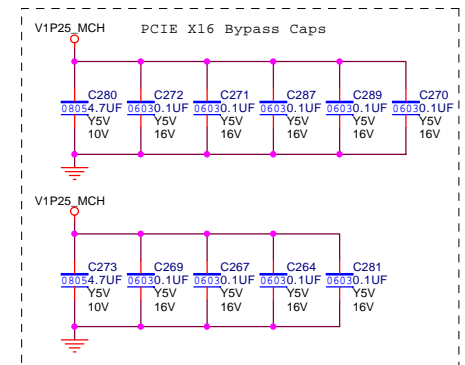
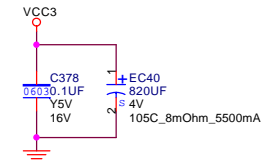
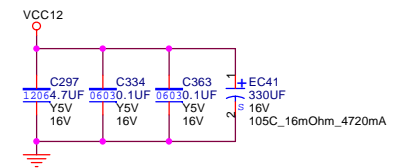
8 SDVO_CTRL_CLK >>

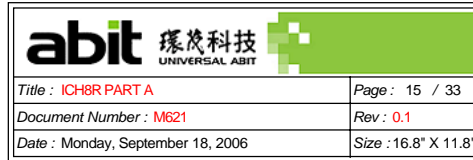
8 SDVO_CTRL_DATA >>

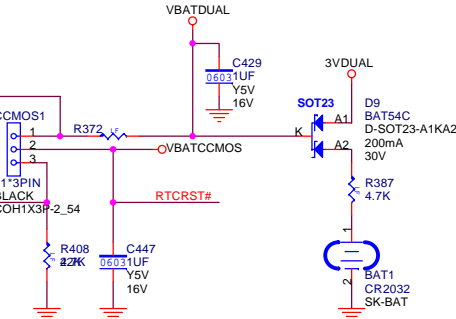
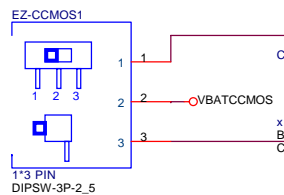
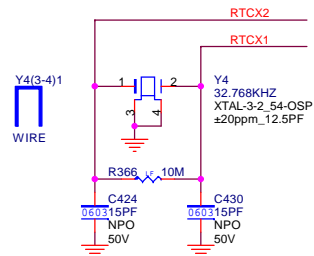
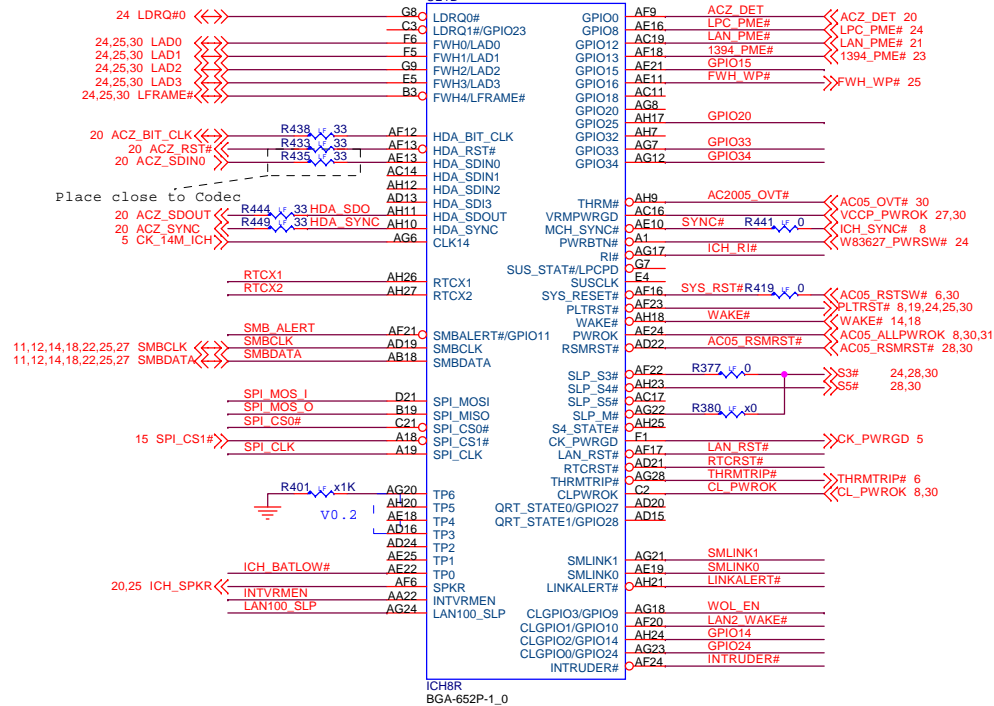
8 EXP_PRSTN <<



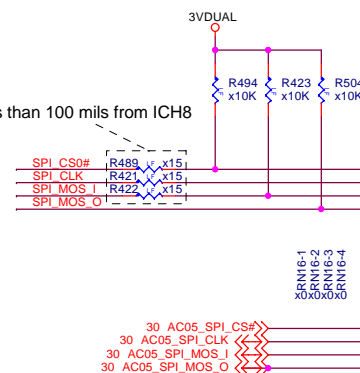
PCIE_RST# <<< PCIE_RST# 18,24
WAKE# >>> WAKE# 16,18
SMBDATA <<< SMBDATA 11,12,16,18,22,25,27
SMBCLK <<< SMBCLK 11,12,16,18,22,25,27



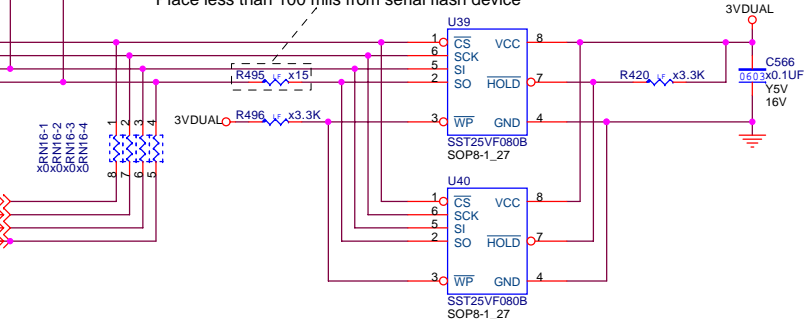




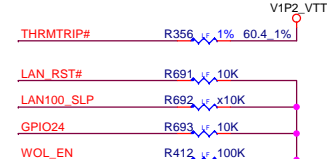
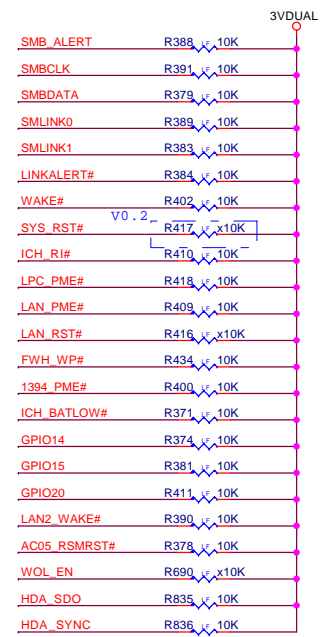
Place less than 100 mils from ICH8

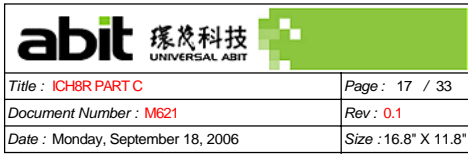


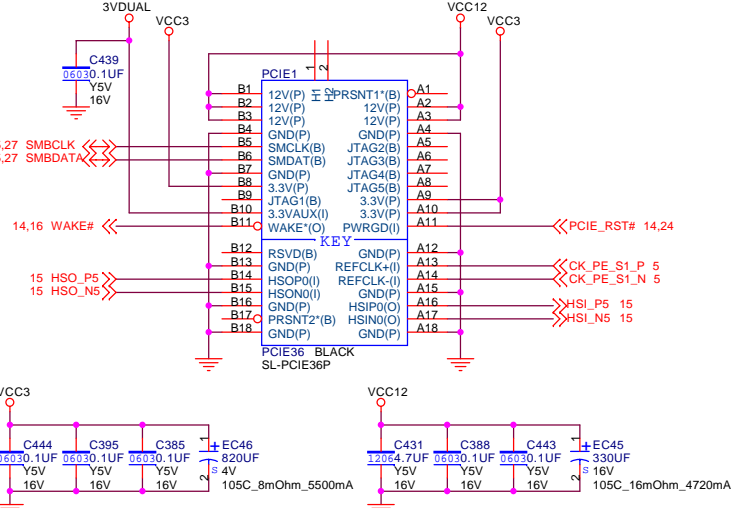
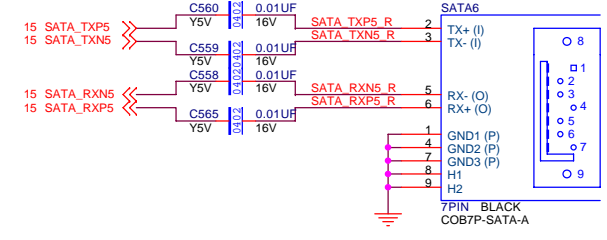
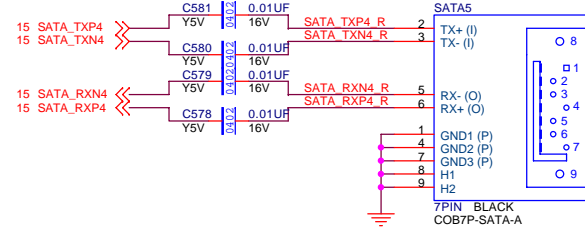
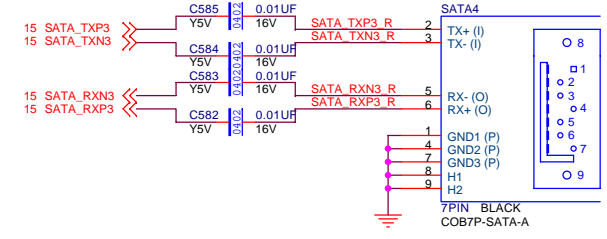
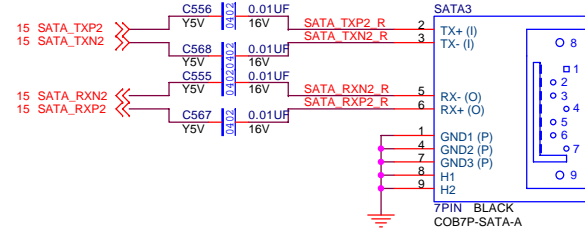
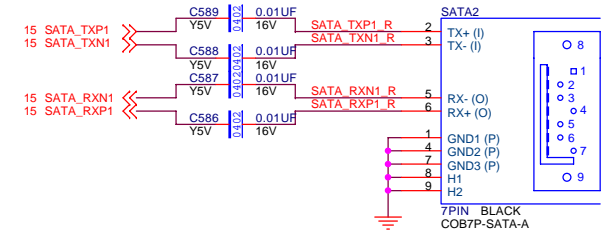
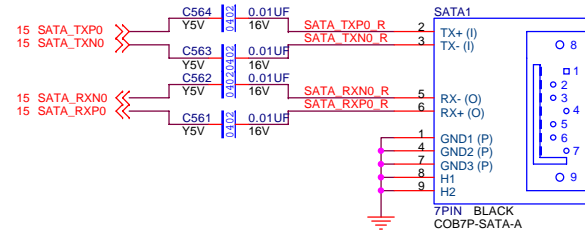
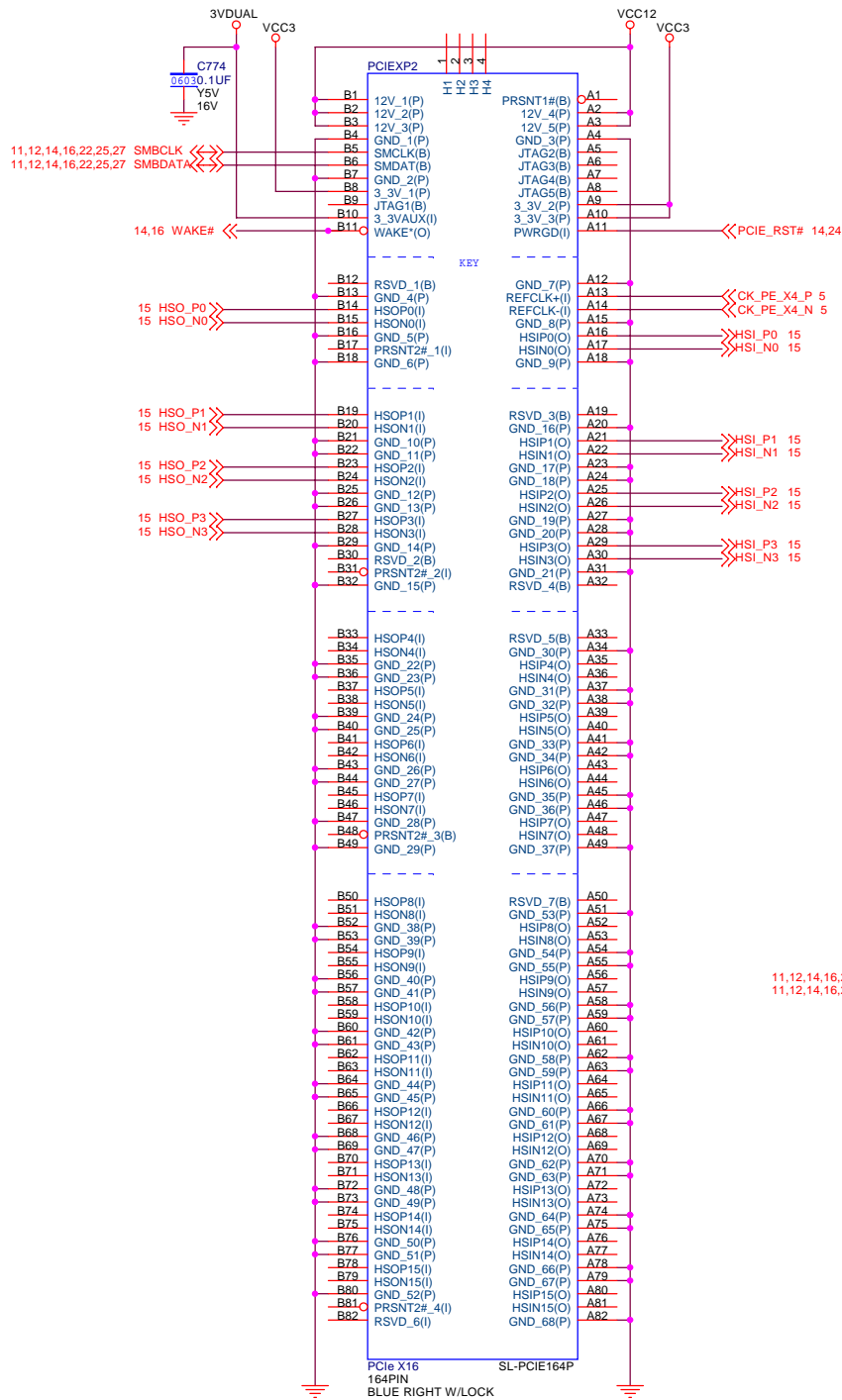
Place less than 100 mils from serial flash device



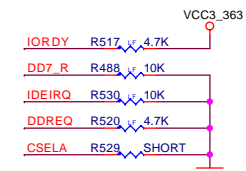
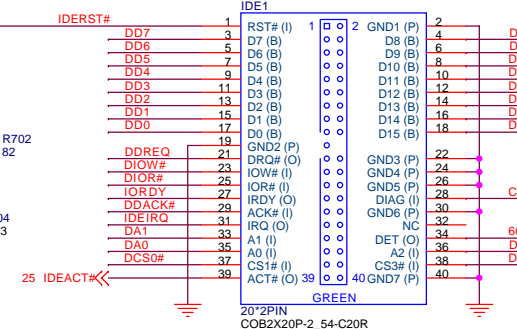
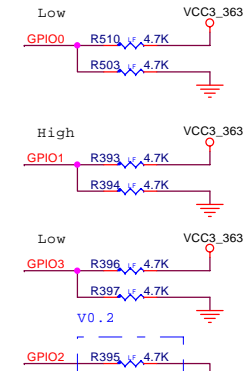
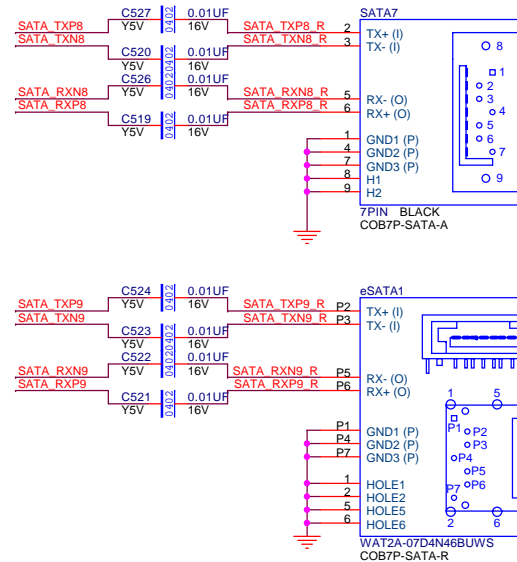
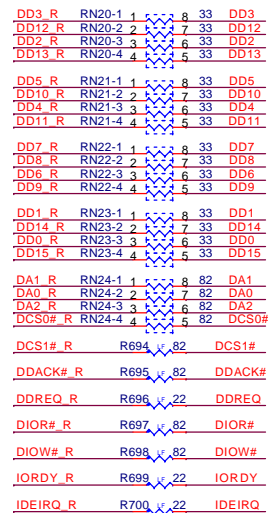
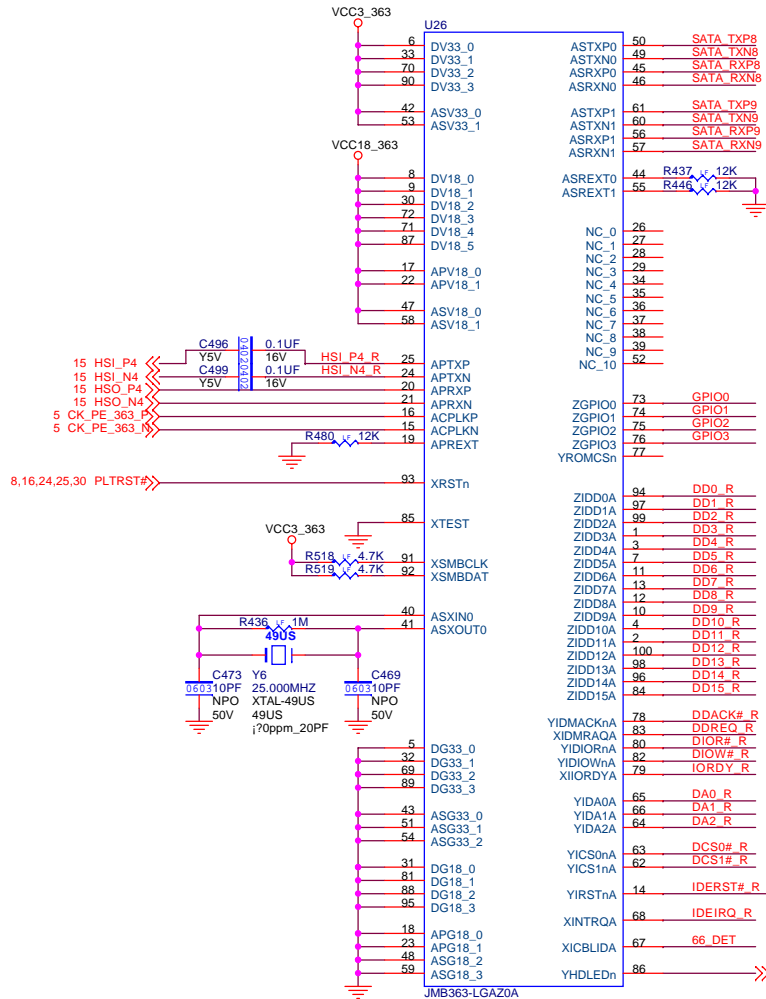
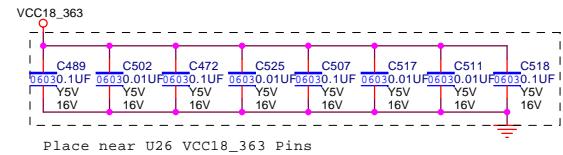
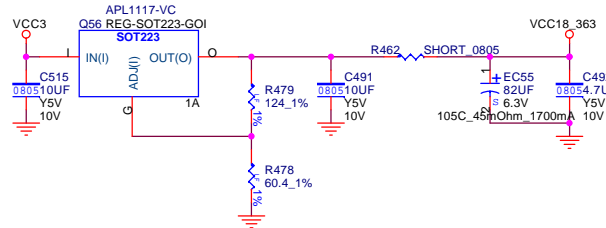
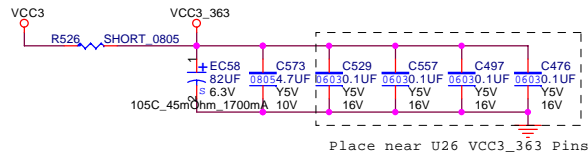
Model	GPIO34	CPIO33
AB9 Pro	0	0
AB9	0	1

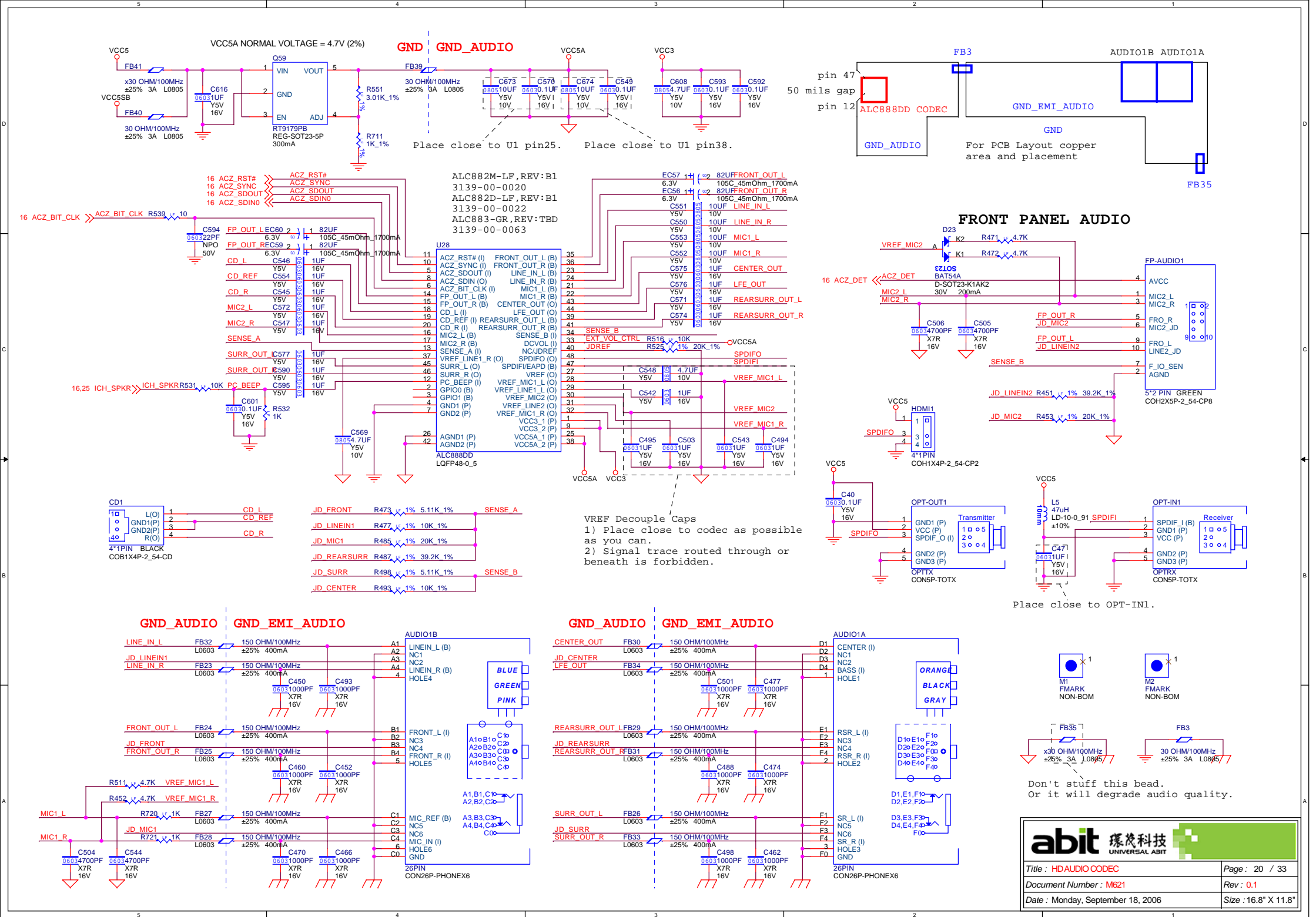


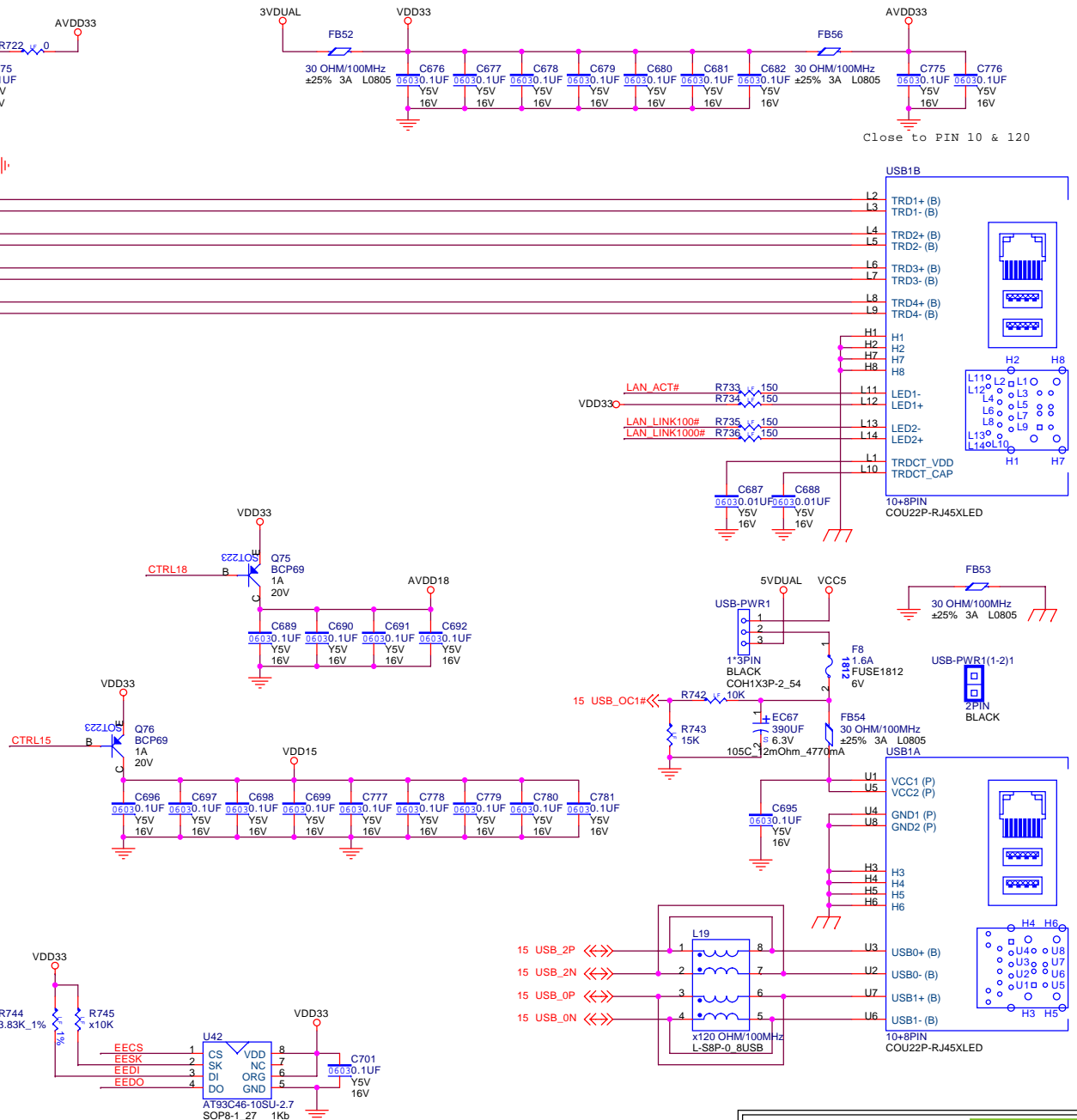
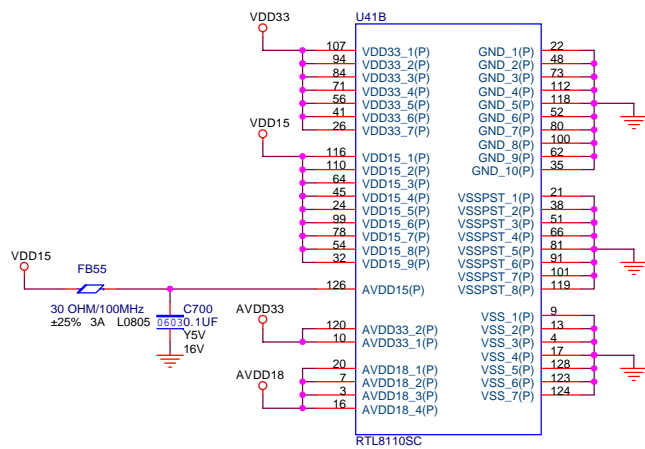
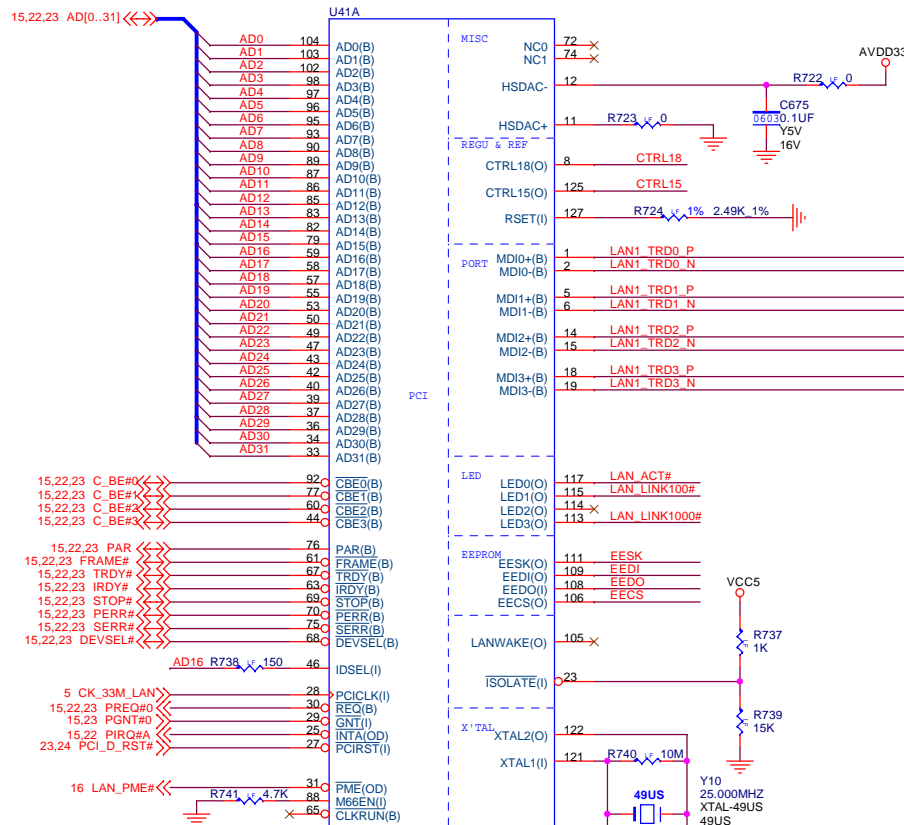




FOR PCI EXPRESS X1 SLOT 1

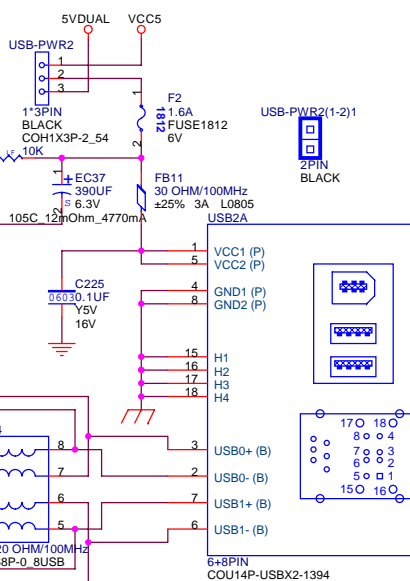
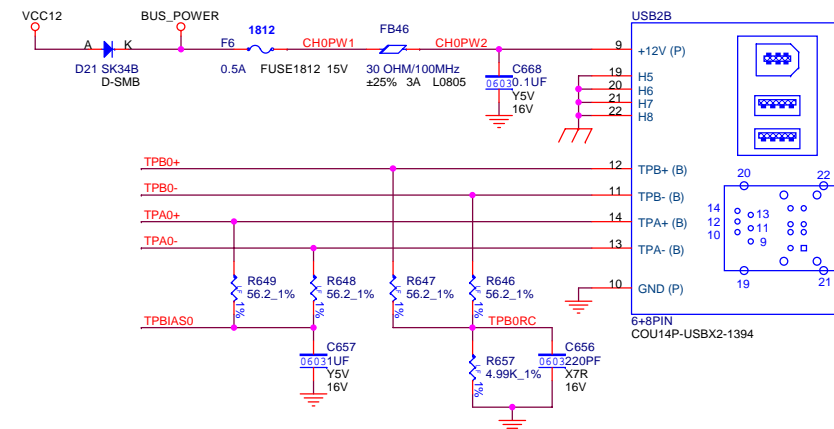




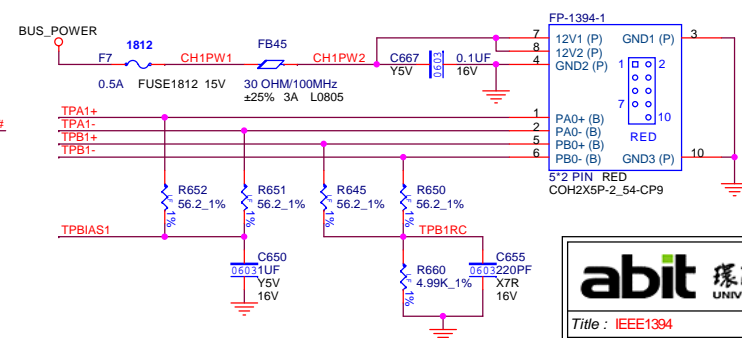




IEEE-1394 Channel 0



IEEE-1394 Channel 1



TSB43AB22

PCI BUS INTERFACE

PHY PORT 2

BIAS CURRENT

OSCILLATOR

FILTER

EEPROM 2 WIRE BUS

POWER CLASS

PHY PORT 1

CYCLEOUT / CARDBUS

GPIO3

GPIO2

GPIO1

GPIO0

GPIO4

GPIO5

GPIO6

GPIO7

GPIO8

GPIO9

GPIO10

GPIO11

GPIO12

GPIO13

GPIO14

GPIO15

GPIO16

GPIO17

GPIO18

GPIO19

GPIO20

GPIO21

GPIO22

GPIO23

GPIO24

GPIO25

GPIO26

GPIO27

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